**METHOD AND SYSTEM
FOR TRIGGERING A DEBUGGING UNIT**

ABSTRACT OF THE DISCLOSURE

A processor core for transitioning a debugging unit between a plurality of operating states in response to an instruction stream is disclosed. The processor core generates trace data as it processes operating signals of the instruction stream. The processor core provides a first trigger event signal to the debugging unit in response to a first trigger instruction signal within the instruction stream that is representative of a triggering instruction to transitions the debugging unit to a base operating state. The processor core provides a second trigger event signal to the debugging unit in response to a second trigger instruction signal within the instruction stream that is representative of a triggering instruction to dynamically store trace data within the memory component of the debugging unit. The processor core provides a third trigger event signal to the debugging unit in response to a third trigger instruction signal within the instruction stream that is representative of a triggering instruction to statically store trace data within the memory component of the debugging unit. Concurrently or alternatively, the processor core can provide one or more of the trigger event signals to the debugging unit as a function of a generated trigger data in response to additional operational instructions within the instruction stream.